CLAIMS:

1. A detector arrangement for detecting a frequency error between an input signal (DATA) and a reference signal, said detector arrangement comprising:

a) first latch means (L1, L2) for sampling a quadrature component (CKQ) of said reference signal based on said input signal, to generate a first binary signal (PD_Q);

b) second latch means (L3, L4) for sampling an in-phase component (CKI) of said reference signal based on said input signal, to generate a second binary signal (PD_I); and

c) third latch means (L5) for sampling said first binary signal based on said second binary signal, to generate a frequency error signal (FD).

2. A detector arrangement according to claim 1, further comprising control means (TS) for selectively suppressing operation of a charge pump circuit (82) to which said first binary signal (PD_Q) is supplied, in response to a control signal derived from said second binary signal.

3. A detector arrangement according to claim 1 or 2, wherein said first and second latch means each comprise a double-edge triggered flip-flop arrangement.

4. A detector arrangement according to claim 3, wherein said double-edge triggered flip-flop arrangement comprises first and second D-latch circuits (L1, L2) receiving said input signal and being respectively controlled by a direct version and an inversed version of the respective component of said reference signal, and a multiplexer circuit (MUX) being controlled by said inversed version of said respective component.

5. A detector arrangement according to any one of the preceding claims, wherein said third latch means comprises a D-latch circuit (L5) receiving said first binary signal (PD_Q) and being controlled by said second binary signal (PD_I).

6. A detector arrangement according to any one of the preceding claims, wherein said reference signal is a clock signal to be recovered from said input signal.

7. A detector arrangement according to claim 2, wherein said first and second binary signals (PD_Q, PD_I) are supplied to said charge pump circuit (82) via at least one of respective amplifier and level shifter circuits (84, 86).

8. A detector arrangement according to claim 7, wherein said amplifier circuits (84) each comprise a combination of a feedback amplifier and a feedforward amplifier.

9. A charge pump circuit for use in a frequency detector arrangement, said charge pump circuit comprising:

a) a differential input circuit having first and second differential branches;

b) modulating means for modulating first and second current sources respectively arranged in said first and second differential branches; and

c) control means for controlling a tail current of said differential input circuit in response to a frequency-locked state of said frequency detector arrangement.

10. A charge pump circuit according to claim 9, further comprising first and second current mirror circuits (CM) respectively provided in said first and second differential branches and arranged to copie the modulated current of one differential branch into the respective other differential branch.

11. A charge pump circuit according to claim 9 or 10, further comprising a common mode rejection means (C) for comparing a common-mode voltage at the output of said charge pump circuit with a reference voltage (V_{CM}), and for controlling said first and second current sources based on the comparison result.

12. A charge pump circuit according to any one of claims 9 to 11, wherein said control means comprises switching means (M1, M2) for switching said tail current in response to a control signal indicating said frequency-locked state.

13. A recovery circuit for recovering timing information for random data, said recovery circuit comprising a detector arrangement according to any one of claims 1 to 8, and

a charge pump circuit according to any one of claims 9 to 12, wherein said frequency error signal generated by said detector arrangement is supplied to said charge pump circuit, and wherein said frequency-locked state is signaled by using said second binary signal generated by said detector arrangement.

14. A method of detecting a frequency error between an input signal and a reference signal, said method comprising the steps of:

a) sampling a quadrature component of said reference signal based on said input signal, to generate a first binary signal;

b) sampling an in-phase component of said reference signal based on said input signal, to generate a second binary signal; and

c) sampling said first binary signal based on said second binary signal, to generate a frequency error signal.

15. A method of controlling a charge pump circuit used in a frequency detection arrangement, said method comprising the steps of:

a) modulating first and second current sources respectively arranged in first and second differential branches of a differential input circuit of said charge pump circuit; and

b) controlling a tail current of said differential input circuit in response to a frequency-locked state of said frequency detector arrangement.